

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Furukawa et al.

Serial No.: 10/767,039

Filed: January 29, 2004

For: VERTICAL FIELD EFFECT TRANSISTORS INCORPORATING SEMICONDUCTING NANOTUBES GROWN IN A SPACER-DEFINED PASSAGE

Cincinnati, Ohio 45202

Art Unit: 2814

Examiner: Phat X. Cao

Atty. Docket No.: ROC920030272US1

Date: April 19, 2006

Commissioner of Patents and Trademarks  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**DECLARATION UNDER RULE 131**

We, Toshiharu Furukawa, Mark Charles Hakey, Steven John Holmes, David Vaclav Horak, Peter H. Mitchell, and Larry Alan Nesbit (the inventors), being duly cautioned and sworn, submit this Declaration in response to the Office Action dated February 9, 2006, and state:

That we are the inventors of the invention entitled "VERTICAL FIELD EFFECT TRANSISTORS INCORPORATING SEMICONDUCTING NANOTUBES GROWN IN A SPACER-DEFINED PASSAGE" described and claimed in the application for Letters Patent of the United States, Serial No. 10/767,039, filed January 29, 2004 ('039 application);

That this is a Declaration under the provisions of Rule 131 and the rules of practice for the United States Patent Office in support of said '039 application;

That the invention described and claimed in the '039 application was conceived prior to September 25, 2003, the publication date of U.S. Patent Application Publication No. 2004/0178617 in the name of Appenzeller et al.;

That, as evidence of the conception of the invention described and claimed in the '039 application, attached and incorporated into this Declaration as Exhibit A are copies of original annotated drawings, which bear dates (now masked), created by one or all of the undersigned inventors in the United States prior to September 25, 2003 and bearing a date before September 25, 2003 (but with said date now masked);

That the attached Exhibit includes a detailed description of a vertical semiconductor device structure, which clearly demonstrates that such vertical semiconductor device structure embodies the elements claimed in at least the independent claims of the '039 application, and which

was conceived prior to the September 25, 2003 publication date of Appenzeller et al.;

That the conception of the invention claimed in at least pending independent claims 1, 42, and 47 of the '039 application is fully supported by the attached Exhibit, and that all annotated drawings and text included in the Exhibit having been created in the United States by one or all of the undersigned inventors before the September 25, 2003 publication date of Appenzeller et al.;

That the Exhibit demonstrates as follows:

That a semiconductor device structure was conceived before September 25, 2003;

That the semiconductor device structure included a substrate defining a substantially horizontal plane; a gate electrode projecting vertically from said substrate and including a vertical sidewall; a spacer of a dielectric material flanking said vertical sidewall and spaced horizontally from said vertical sidewall of said gate electrode to define a vertical passage, said spacer extending vertically relative to said gate electrode such that said passage has a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode; a semiconducting nanotube extending between opposite first and second ends with a substantially vertical orientation; a spacer of a dielectric material flanking said vertical sidewall and spaced horizontally from said vertical sidewall of said gate electrode to define a vertical passage having horizontal dimensions appropriate for the synthesis of said semiconducting nanotube, said semiconducting nanotube positioned in said vertical passage, and said spacer extending vertically relative to said gate electrode such that said vertical passage a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode; a gate dielectric disposed on said vertical sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube;

That the semiconductor device structure may have alternatively included a substrate; a gate electrode projecting from said substrate and including a sidewall; a first spacer of a dielectric material flanking said sidewall to define a passage; a semiconducting nanotube positioned in said passage between said sidewall and said spacer and extending between opposite first and second ends; a gate dielectric disposed on said sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source;

That the semiconductor device structure may have alternatively included a gate electrode projecting from a substrate and including a sidewall; a first spacer of a dielectric material flanking said sidewall of said gate electrode to define a passage; a semiconducting nanotube positioned in said passage between said sidewall of said gate electrode and said spacer, said semiconducting nanotube extending between opposite first and second ends; a gate dielectric disposed on said sidewall of said gate electrode between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source, and said semiconducting nanotube having a length such that said second end of said semiconducting nanotube projects beyond said gate electrode and into said drain;

as called for in the pending independent claims in the ‘039 application;

That the undersigned inventors were diligent from prior to the publication date of September 25, 2003, which represents the publication date of U.S. Patent Application Publication No. 2004/0178617, to January 29, 2004, which represents the filing date of the ‘039 application. Specifically, the undersigned inventors can account for the entire period during which reasonable diligence is required with affirmative acts within the United States and acceptable excuses. During this period, the attorneys acted within the United States with reasonable diligence on the application. Specifically, in-house counsel for the Assignee was diligent in reviewing the attached Exhibit prepared by the inventors and forwarding the attached Exhibit to outside counsel for the Assignee on July 15, 2003. Outside counsel for the Assignee was diligent in drafting a specification the ‘039 application and forwarding a draft specification to the inventors on October 21, 2003. In particular, outside counsel for the Assignee had a reasonable backlog of unrelated cases taken up in chronological order and carried out expeditiously. The inventors were diligent in reviewing and approving the draft specification between October 21, 2003 and November 4, 2003. Outside counsel for the Assignee was diligent in finalizing the specification of the ‘039 application, after receiving comments from the inventors’ review, and forwarding the finalized specification to in-house counsel for the Assignee on November 4, 2003. In-house counsel for the Assignee was diligent in forwarding the specification for the ‘039 application and a Declaration/Power of Attorney to the inventors and, subsequently, filing the ‘039 application and the executed Declaration/Power of Attorney at the U.S. Patent and Trademark Office on January 29, 2004;

Therefore, in summary, the Declaration and attached Exhibit constitute a showing of facts, in character and weight, that establish conception of the invention prior to the publication date of U.S. Patent Application Publication No. 2004/0178617 for a semiconductor device structure that is the subject of and is claimed in Application Serial No. 10/767,039, all the acts of which occurred in the United States BEFORE September 25, 2003, and thus precede the publication date of U.S. Patent Application Publication No. 2004/0178617, and that the inventors and counsel for the inventors exhibited diligence from prior to the publication date of September 25, 2003 to the filing date of the '039 application.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Further declarants sayeth naught.

By   
Toshiharu Furukawa

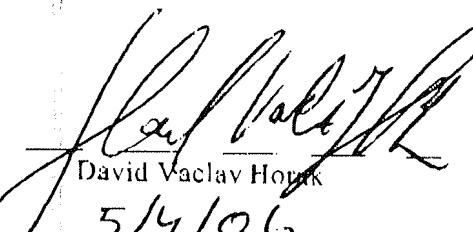
Date 5/4/2006

By \_\_\_\_\_  
Mark Charles Hickey

Date \_\_\_\_\_

By   
Steven John Holmes

Date 5/4/2006  
*SJH*

By   
David Vaclav Horak

Date 5/4/06

By \_\_\_\_\_  
Peter H. Mitchell

Date \_\_\_\_\_

By \_\_\_\_\_  
Larry Alan Nesbit

Date \_\_\_\_\_

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By \_\_\_\_\_  
Toshiharu Furukawa

Date \_\_\_\_\_

By \_\_\_\_\_  
Mark Charles Hakey

Date \_\_\_\_\_

By \_\_\_\_\_  
Steven John Holmes

Date \_\_\_\_\_

By \_\_\_\_\_  
David Vaclav Horak

Date \_\_\_\_\_

By Peter H. Mitchell  
Peter H. Mitchell

Date April 19, 2006

By \_\_\_\_\_  
Larry Alan Nesbit

Date \_\_\_\_\_

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Further declarants sayeth naught.

By \_\_\_\_\_  
Toshiharu Furukawa

Date \_\_\_\_\_

By Mark Charles Hakey  
Mark Charles Hakey

Date 65/05/2006

By \_\_\_\_\_  
Steven John Holmes

Date \_\_\_\_\_

By \_\_\_\_\_  
David Vaclav Horak

Date \_\_\_\_\_

By \_\_\_\_\_  
Peter H. Mitchell

Date \_\_\_\_\_

By \_\_\_\_\_  
Larry Alan Nesbit

Date \_\_\_\_\_

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By \_\_\_\_\_  
Toshiharu Furukawa

Date \_\_\_\_\_

By \_\_\_\_\_  
Mark Charles Hakey

Date \_\_\_\_\_

By \_\_\_\_\_  
Steven John Holmes

Date \_\_\_\_\_

By \_\_\_\_\_  
David Vaclav Horak

Date \_\_\_\_\_

By \_\_\_\_\_  
Peter H. Mitchell

Date \_\_\_\_\_

By Larry Alan Nesbit  
Larry Alan Nesbit  
Date April 20, 2006

EXHIBIT A

**Disclosure ROC8-2003-0269**

Prepared for and/or by an IBM Attorney - IBM Confidential



Created By Larry Nesbit On  
Last Modified By Larry Nesbit

Required fields are marked with the asterisk (\*) and must be filled in to complete the form .

**\*Title of disclosure (in English)**

Carbon NanoTubes (CNT) Grown in a Spacer-Defined Channel to Form Vertical FETs.

### **\*Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

The problems solved by this invention are:

1. The controlled growth of carbon nanotubes (CNTs) in a well-defined direction (vertical) to form vertical FET CNTs;

2. Easy access of the reactant gases to the catalyst/CNT growth interface.

The intended growth of the CNTs is to form the semiconductor portion of a vertical transistor.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

The key structure of the invention is the formation of a spacer, separated (by a finite, controlled distance) from a conductor in the vertical direction, and from the substrate in the horizontal direction. The vertical separation provides a narrow gap in which semiconducting carbon nanotubes are grown, thereby confining their growth in the vertical direction. The separation of the spacer from the substrate in the horizontal direction allows for the reactant gases used to form the CNTs to easily diffuse to the CNT/catalyst interface where the growth of the CNT occurs.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

The following is a preferred embodiment of the process used to form this structure for building vertical FET CNTs.

1. On a substrate comprised in part of a top dielectric or insulating material, e.g. SiO<sub>2</sub>, deposit a catalytic material used in the growth of semiconducting carbon nanotubes (CNTs). Such a catalytic material may be, but is not limited to, compounds of nickel (Ni), cobalt (Co), and iron (Fe). See Fig. 1, which shows both a top view and a cross-sectional view of the defined catalytic material. The catalytic material could also be formed on predefined areas of Si isolated by a planarized dielectric material, e.g. SiO<sub>2</sub>. These predefined Si areas would be defined by an AA or RX mask, typically used to define areas of isolation in a Si substrate.

#### Spacer-Defined Nanotube Channel

Deposit, mask, & etch a catalytic material on a substrate.

The catalytic material may be electrically contacted within the substrate. This contact is not shown.

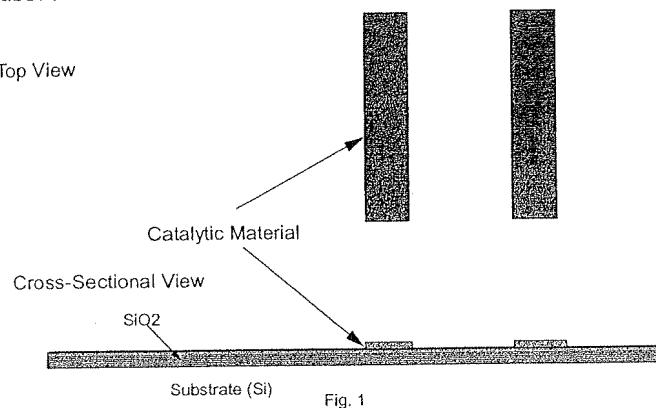


Fig. 1

2. Deposit a thin insulating material, e.g. SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>, over the patterned catalytic material. See Fig. 2.
3. Deposit, mask, and etch a conducting layer, e.g. doped poly-crystalline silicon. The defined poly-Si layer should overlap the defined catalyst layer. See Fig. 2. In order to obtain vertical sidewalls on the poly-Si layer, a hardmask, e.g. SiO<sub>2</sub> and/or Si<sub>3</sub>N<sub>4</sub> may need to be deposited on the poly-Si prior to etching. All or part of the hardmask needs to remain on the poly-Si layer to act as an insulator between the poly-Si and the contacts later in the process.

Spacer-Defined Nanotube Channel

Deposit a thin insulating film, e.g. SiO<sub>2</sub> over the patterned catalytic material.

Deposit, mask, & etch a layer of polycrystalline-Si and an insulating hardmask, overlapping the catalytic material.

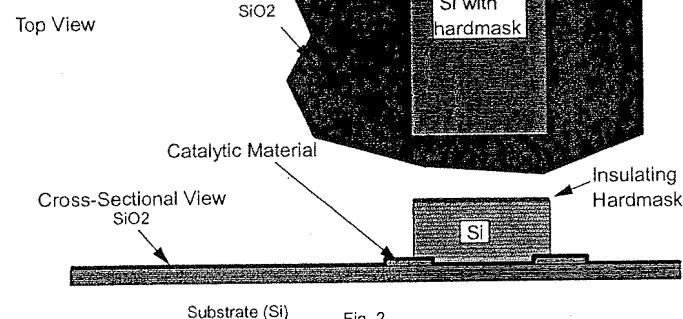


Fig. 2

4. Deposit and etch a thin material film (e.g. SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>) of a controlled thickness to form Spacer 1. See Fig. 3.

Spacer-Defined Nanotube Channel

Deposit and etch a thin film, e.g. SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>, to form spacer 1.

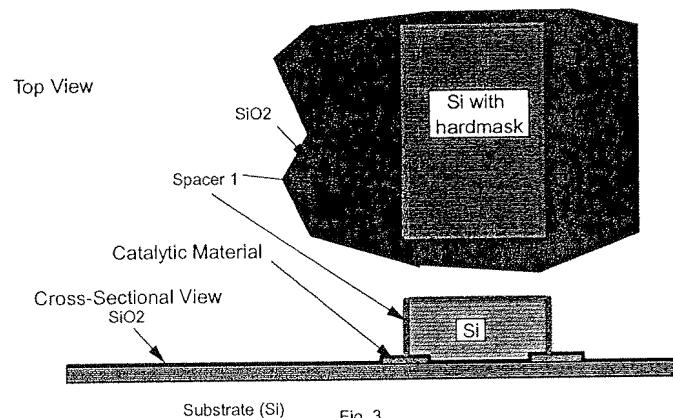
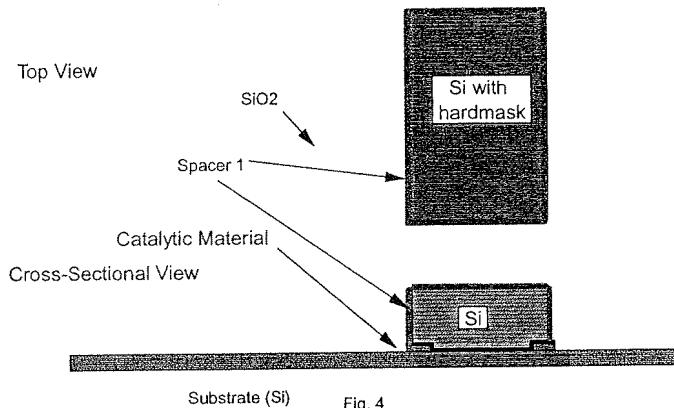


Fig. 3

5. Use spacer 1 as an etch mask to etch the insulator over the catalytic material and to etch the catalytic material to the underlying substrate. See Fig. 4.

#### Spacer-Defined Nanotube Channel

Use spacer 1 to etch the insulator / oxide over the catalytic material and the catalytic material.



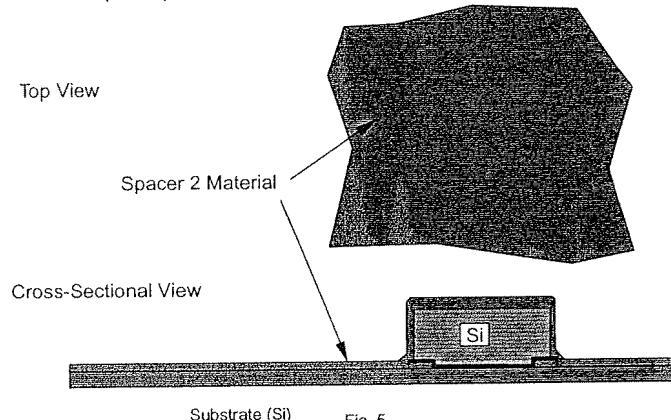
6. Selectively strip / etch spacer 1. See Fig. 5.

7. Deposit another material (e.g. SiO<sub>2</sub> or Ge) that will eventually be formed into an "L-shaped" spacer, spacer 2. See Fig. 5.

#### Spacer-Defined Nanotube Channel

1. Strip the spacer 1.

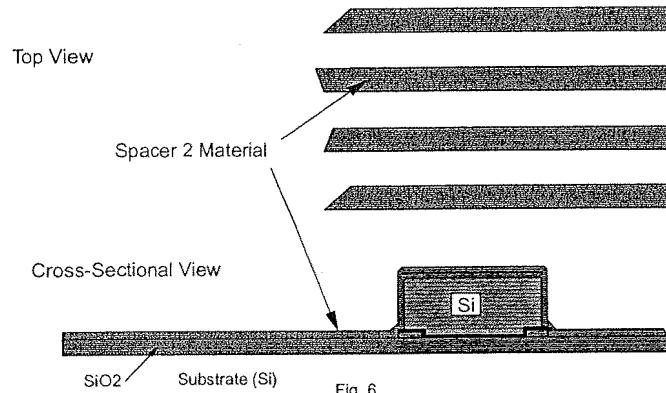
2. Deposit another material that will eventually be formed into an L-shaped spacer 2. This material may be SiO<sub>2</sub> or Ge.



8. Etch the poly-Si / conductor block into smaller rectangles, at or near the minimum lithographic dimensions. See Fig. 6. It should be noted that spacer 2 will be on two of the opposite sides of the poly-Si block, but not on the other two sides of the poly-Si block, where the etch occurred.

### Spacer-Defined Nanotube Channel

Etch the Si block into smaller rectangles, at or near minimum lithographic dimensions.



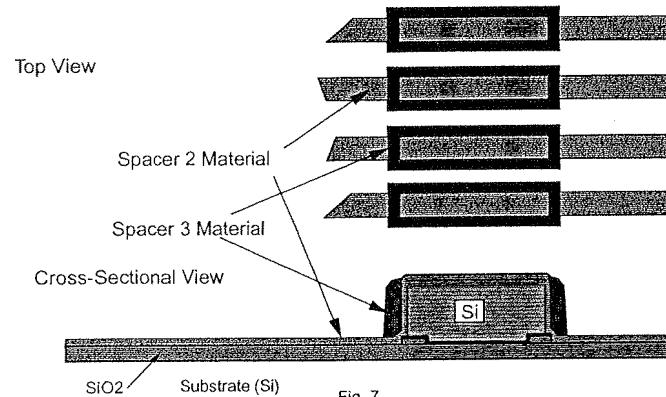
9. Deposit a third spacer material, e.g. Si<sub>3</sub>N<sub>4</sub>, that will be used to form a permanent spacer. See Fig. 7.

10. Etch this material to form spacer 3. See Fig. 7.

### Spacer-Defined Nanotube Channel

Deposit a third spacer material (e.g. Si<sub>3</sub>N<sub>4</sub>) that will be used as a permanent spacer.

Etch this material to form a spacer.



11. Etch the spacer 2 material, using spacer 3 as an etch mask. Note: The hardmask on top of the etch Si block should remain in place. See Fig. 8.

#### Spacer-Defined Nanotube Channel

Etch Spacer 2 by means of an isotropic etch; and etch the insulator covering the catalytic material.

Note that although Spacer 3 appears to be suspended in mid-air in the cross-section, it is attached to the sides or the Si block, in and out of the plane of the paper.

Grow a thin gate oxide on the Si block, without growing oxide on the catalytic material.

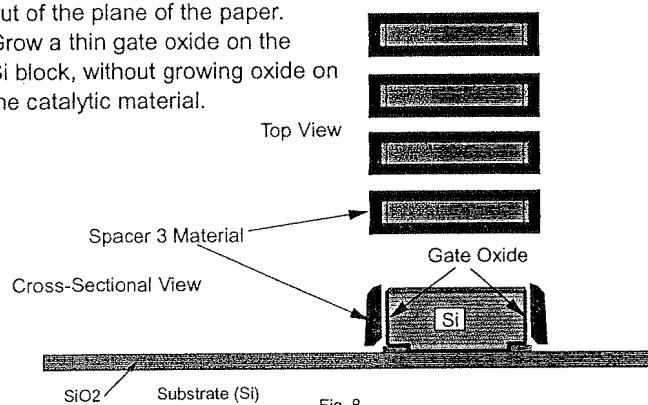


Fig. 8

12. Grow semiconductor-type CNTs from the catalytic material. See Fig. 9. The reactants for the CNT growth could feed the CNT reaction at the catalyst/CNT interface through the space under spacer 3.

#### Spacer-Defined Nanotube Channel

Grow semiconductor-type carbon nanotubes (CNT) from the catalytic material.

The reactants could feed the CNT reaction at the catalytic material through the space under spacer 3.

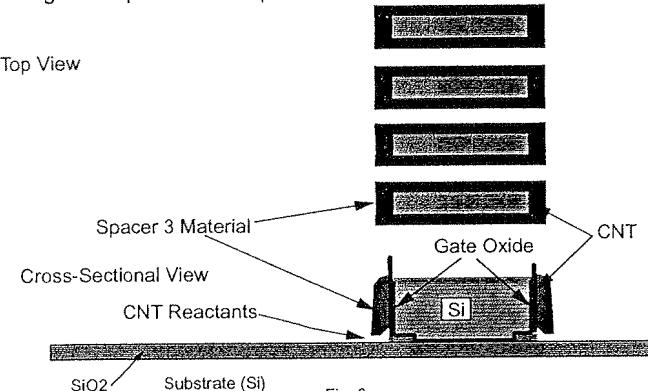
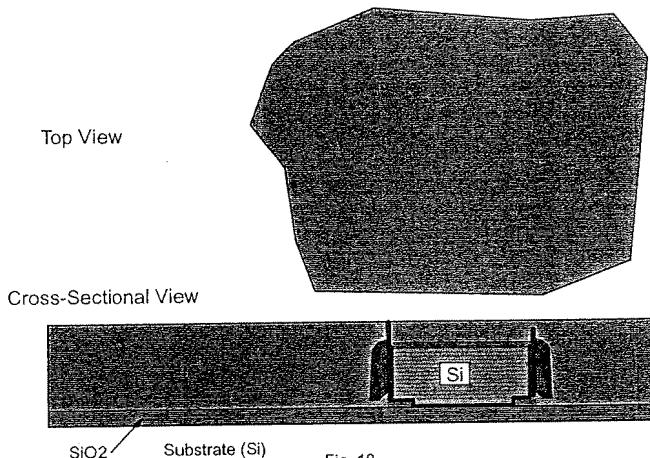


Fig. 9

13. Deposit and planarize an insulating film, e.g. BPSG over the structures in Fig. 9. See Fig. 10.

#### Spacer-Defined Nanotube Channel

Deposit and planarize an insulating film, e.g. BPSG.

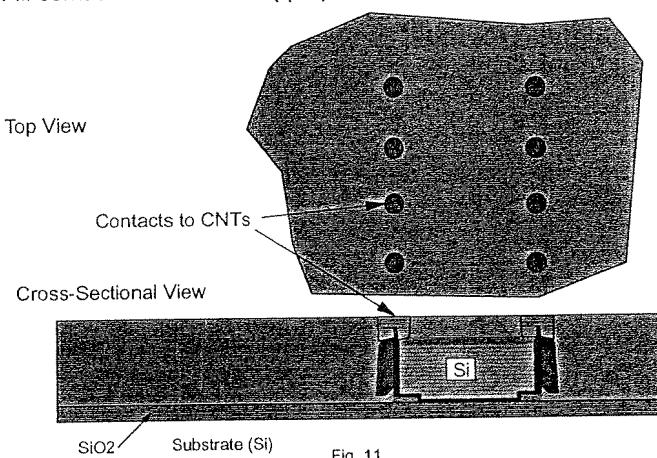


14. Etch contact holes in the BPSG to contact the tops of the CNTs. See Fig. 11. This etch should etch BPSG selective to the hardmask on top of the poly-Si layer. Another contact mask would probably be used to open contacts to the poly-Si layer, as contact holes would have to be made in the BPSG and in the poly-Si hardmask. This latter mask might also be used to etch contacts down to the catalytic material not covered by the poly-Si in other areas of the chip. Fill the contact holes with an appropriate metal/conductor and planarize.

#### Spacer-Defined Nanotube Channel

Etch contact holes to contact the tops of the CNTs.

Fill contact holes with an appropriate metal/conductor & planarize.

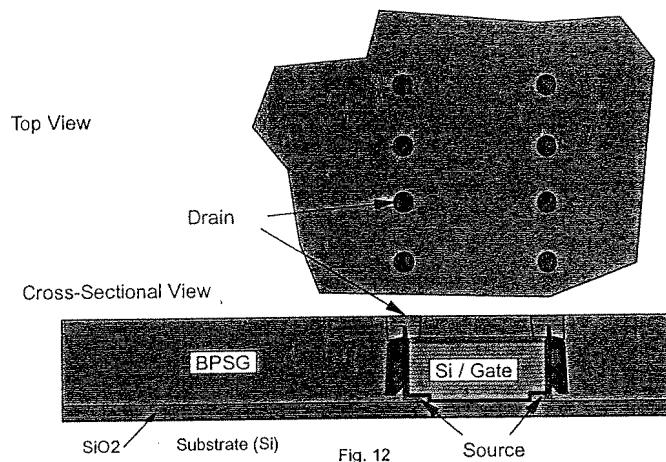


In this manner a vertical CNT FET is formed using:

- the CNT as the semiconducting material;
- the poly-Si layer as the FET gate;
- the catalytic material as the source; and
- the upper contact to the CNT as the FET drain.

See Fig. 12.

Spacer-Defined Nanotube Channel  
Vertical Carbon Nanotube FET



The file containing all of the above schematics is attached below:



CNT within spacer.PRG

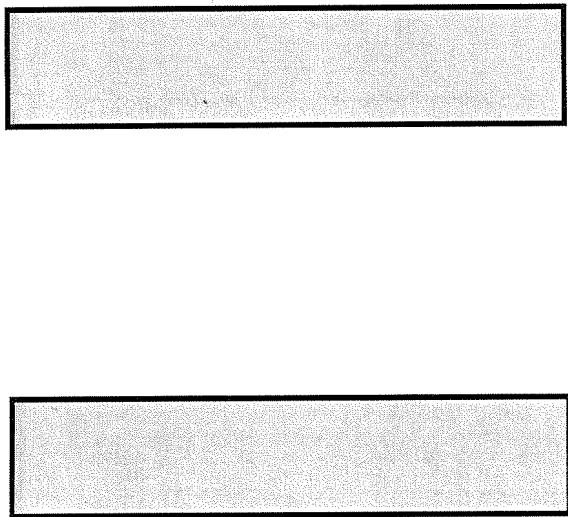
What is claimed is:

1. The formation of a sublithographic vertical channel; the "width" of which is defined by the thickness of a spacer film.
2. The formation of a vertical channel with a horizontal opening at the bottom of the channel in at least one direction.
3. The growth of semiconductor nanotube(s) up the vertical channel from a nucleation (catalyst) site at the base of the vertical channel.
4. The horizontal opening used to allow the flow of gaseous reactants to flow to the catalyst at the base of the vertical channel
5. The formation of a FET device using the semiconductor CNT; the poly-Si (or other conductor) for the gate; the catalyst for the source; and a contact at the other end of the CNT for the drain.

## Spacer-Defined Nanotube Channel

Deposit, mask, & etch a catalytic material on a substrate. The catalytic material may be electrically contacted within the substrate. This contact is not shown.

Top View



Catalytic Material

Cross-Sectional View

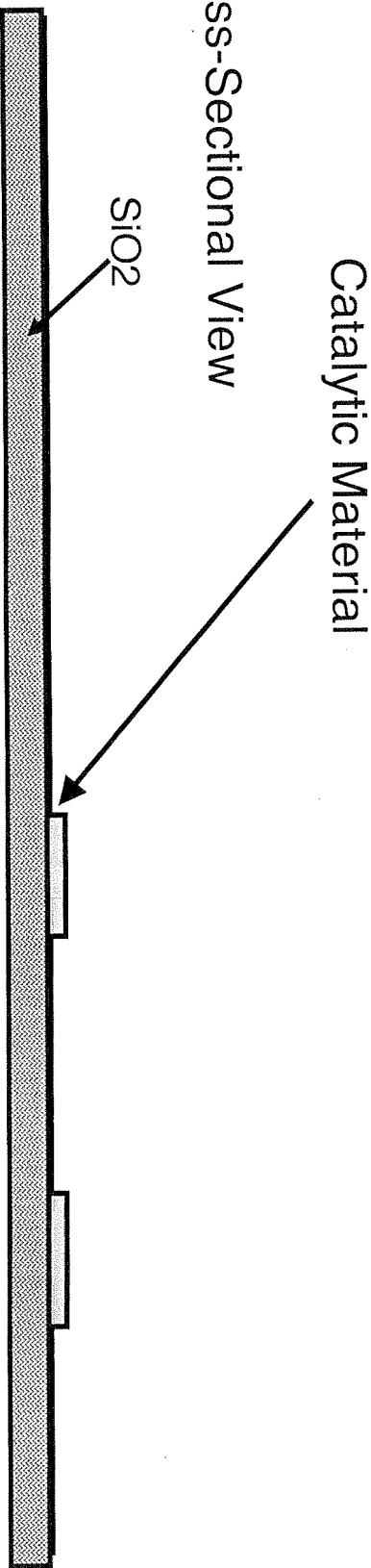


Fig. 1

## Spacer-Defined Nanotube Channel

Deposit a thin insulating film, e.g. SiO<sub>2</sub> over the patterned catalytic material.

Deposit, mask, & etch a layer of polycrystalline-Si and an insulating hardmask, overlapping the catalytic material.

Top View

SiO<sub>2</sub>

Si with  
hardmask

Catalytic Material

Cross-Sectional View

SiO<sub>2</sub>

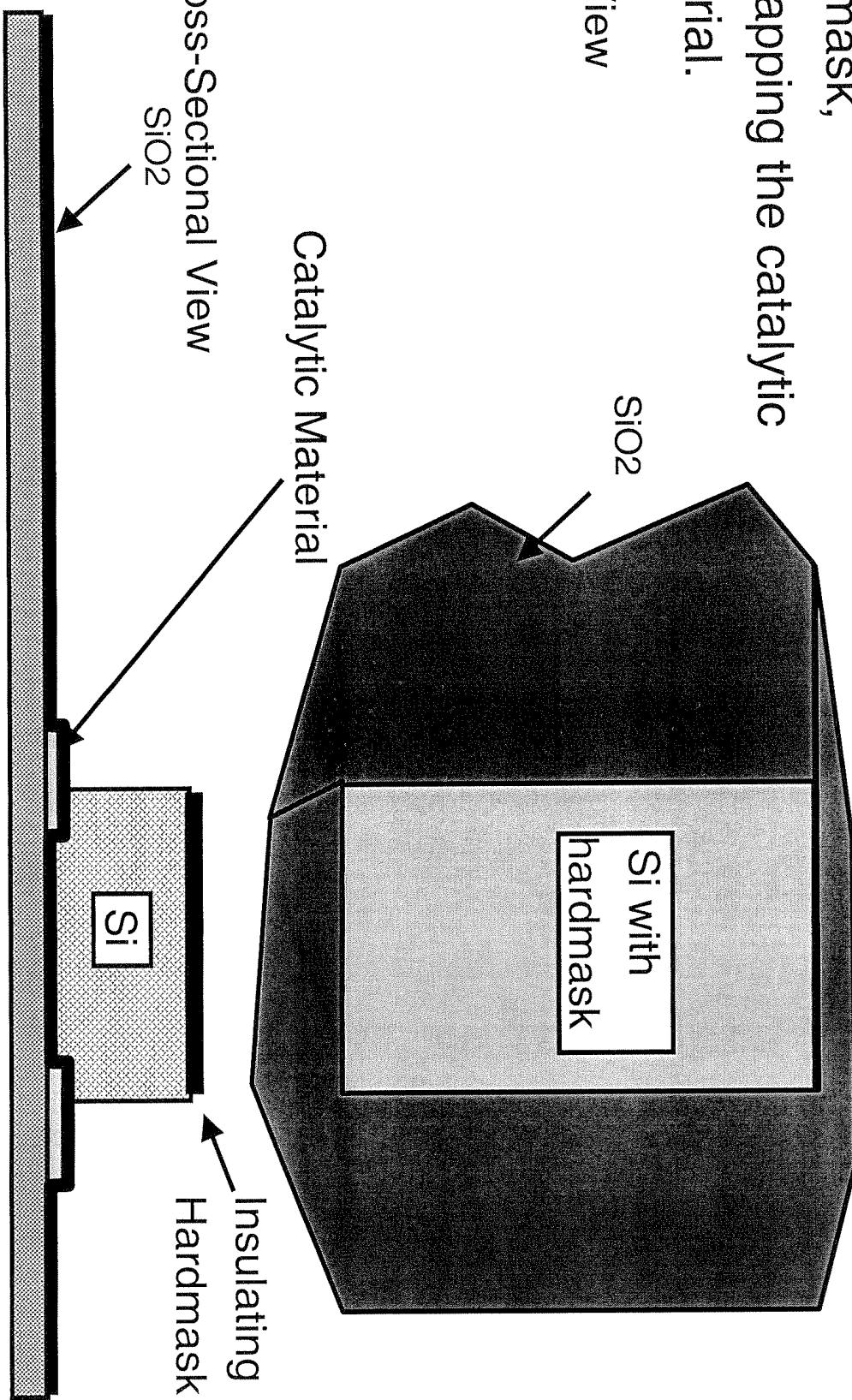


Fig. 2

## Spacer-Defined Nanotube Channel

Deposit and etch a thin film, e.g. SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>, to form spacer 1.

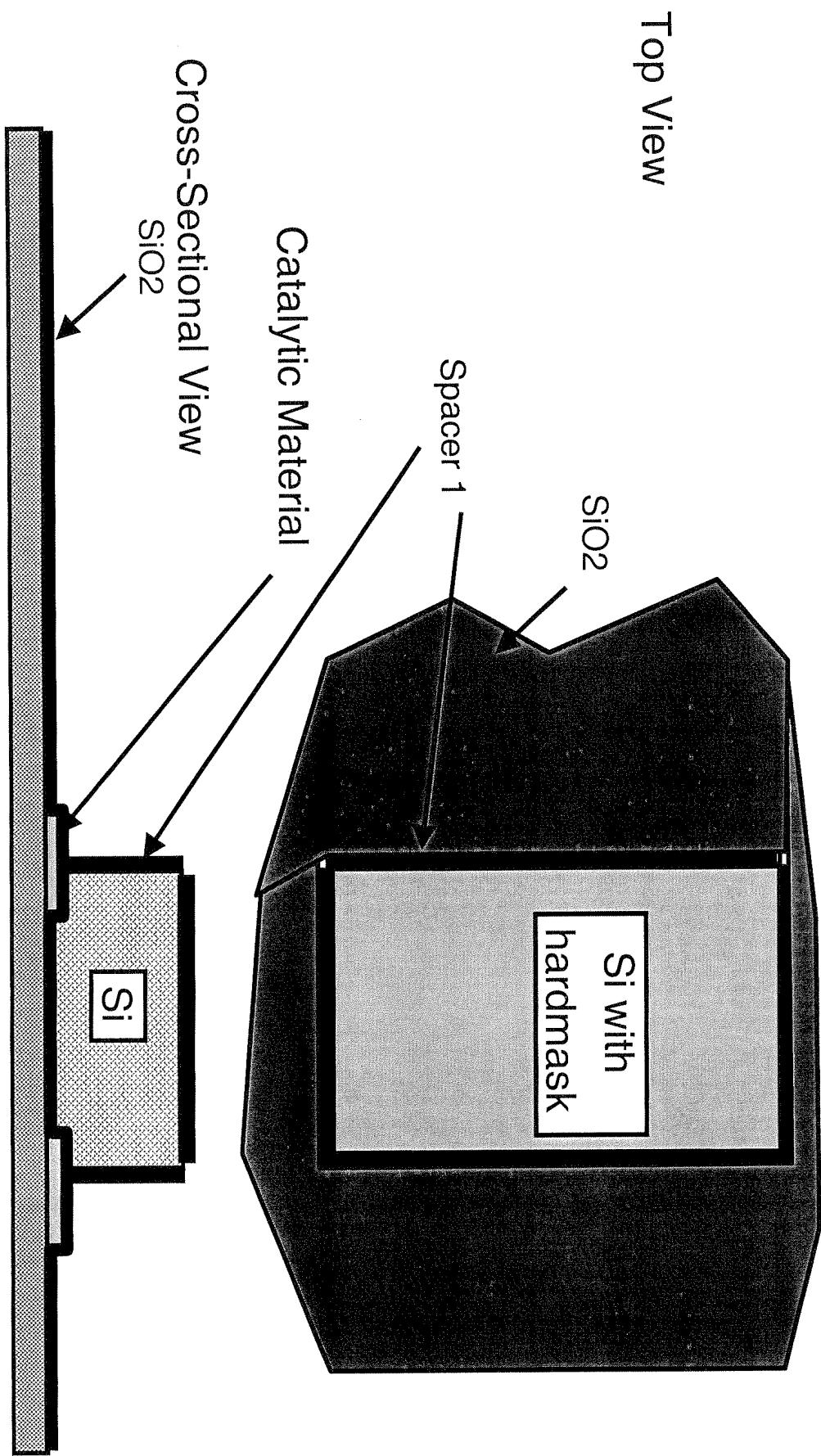
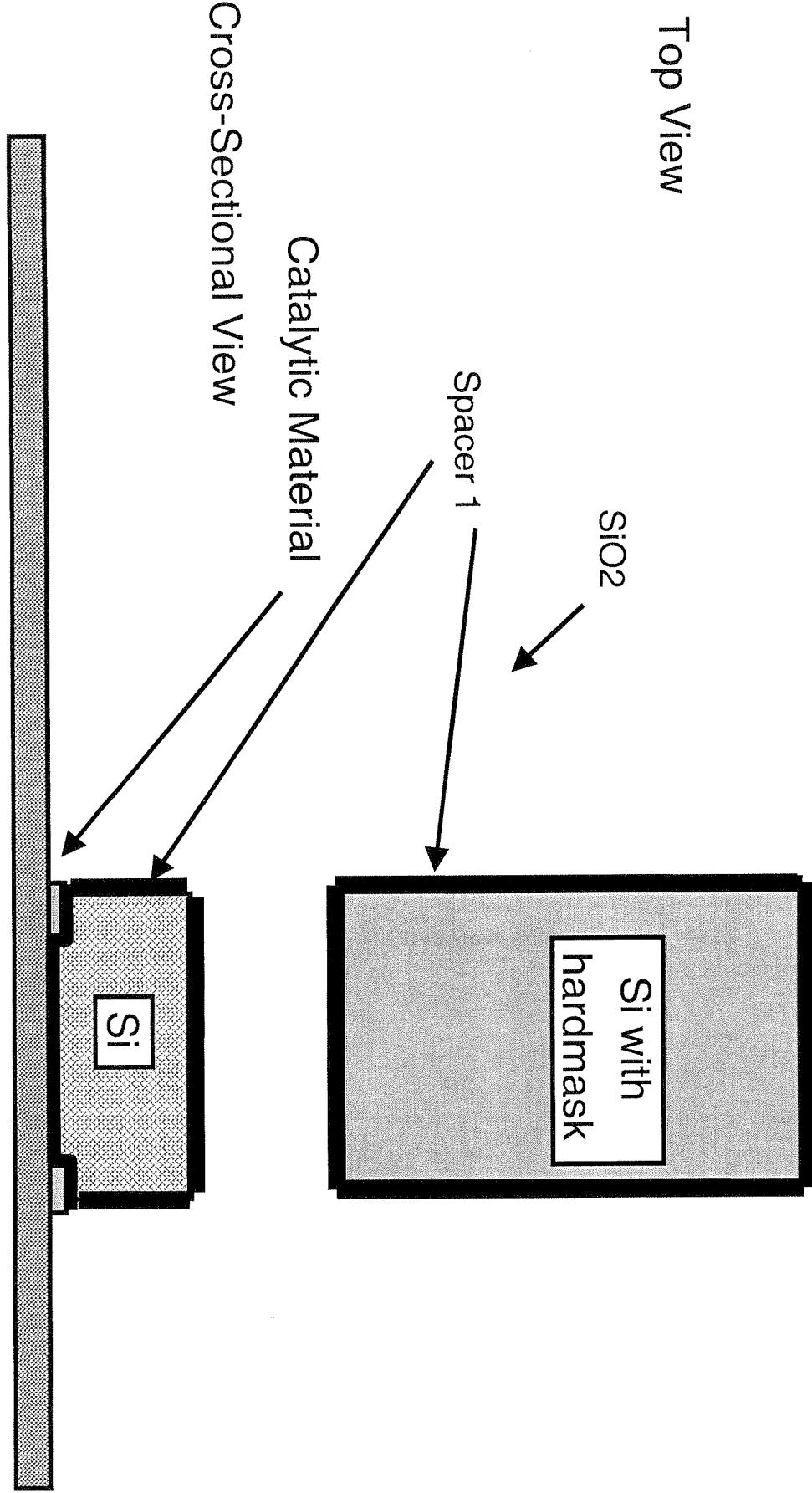


Fig. 3

## Spacer-Defined Nanotube Channel

Use spacer 1 to etch the insulator / oxide over the catalytic material and the catalytic material.

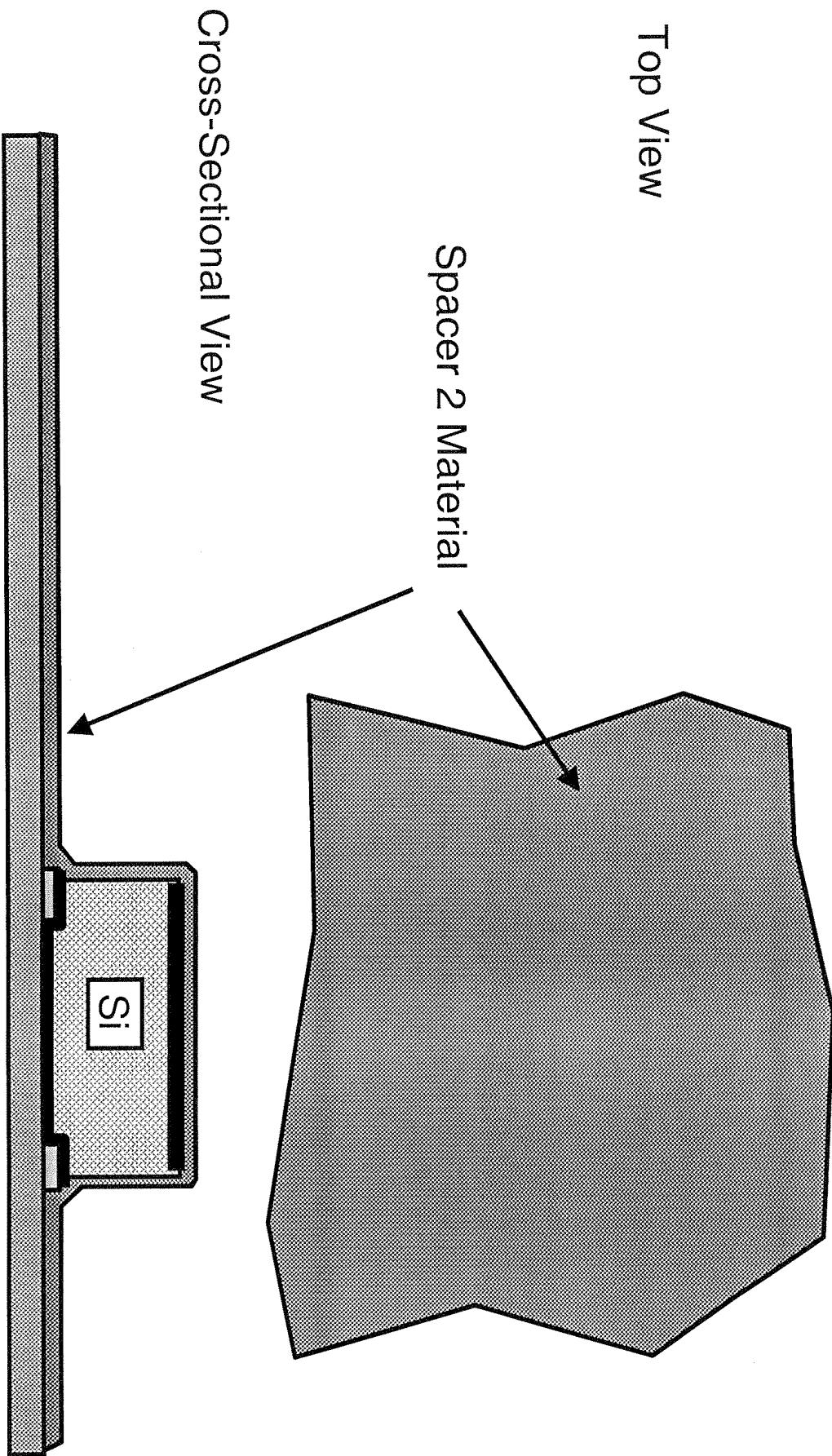


Substrate (Si)

Fig. 4

## Spacer-Defined Nanotube Channel

1. Strip the spacer 1.
2. Deposit another material that will eventually be formed into an L-shaped spacer 2. This material may be SiO<sub>2</sub> or Ge.



Substrate (Si)      Fig. 5

## Spacer-Defined Nanotube Channel

Etch the Si block into smaller rectangles, at or near minimum lithographic dimensions.

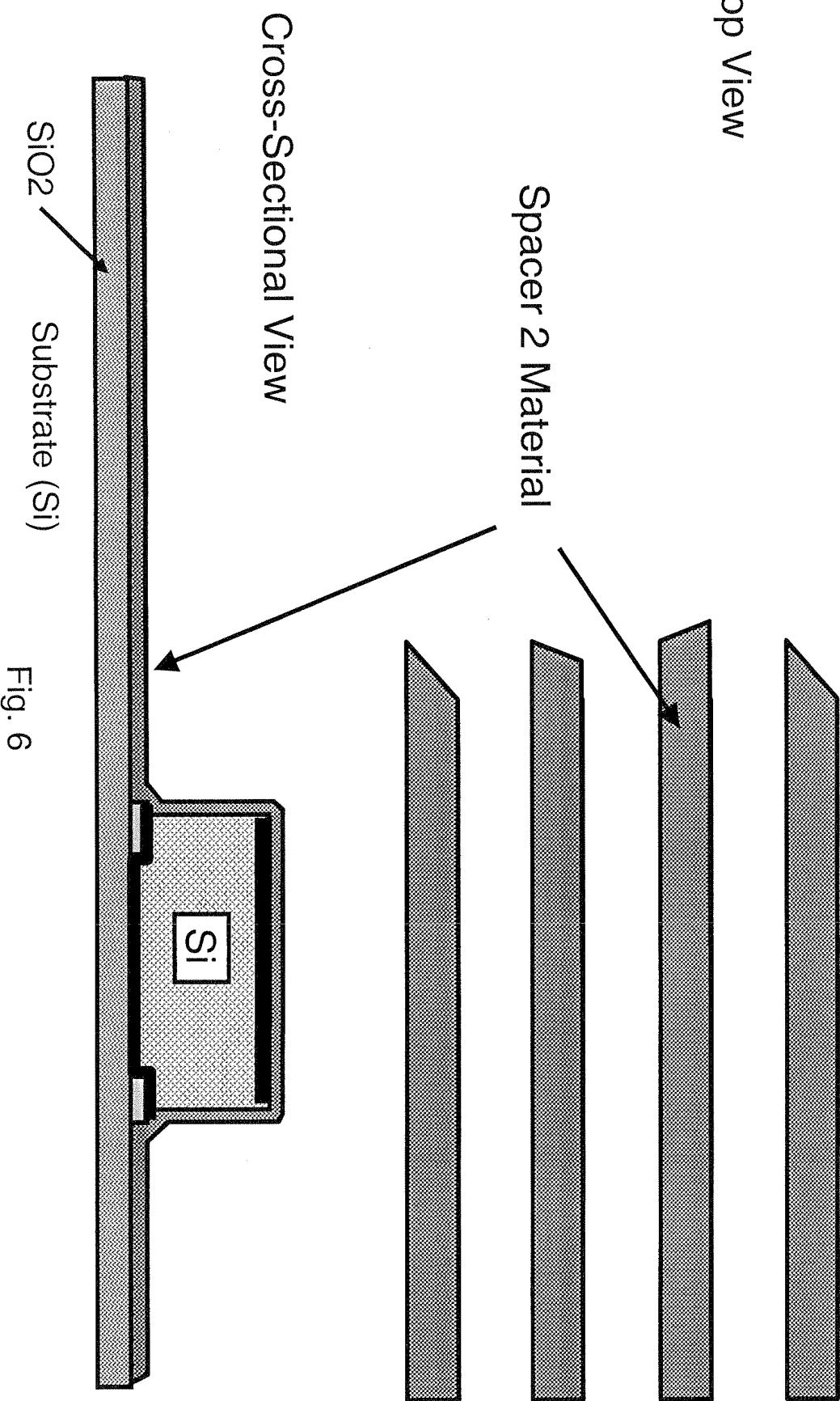


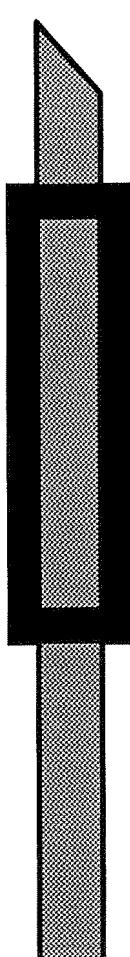
Fig. 6

## Spacer-Defined Nanotube Channel

Deposit a third spacer material (e.g. Si<sub>3</sub>N<sub>4</sub>) that will be used as a permanent spacer.

Etch this material to from a spacer.

Top View



Spacer 2 Material

Spacer 3 Material

Cross-Sectional View

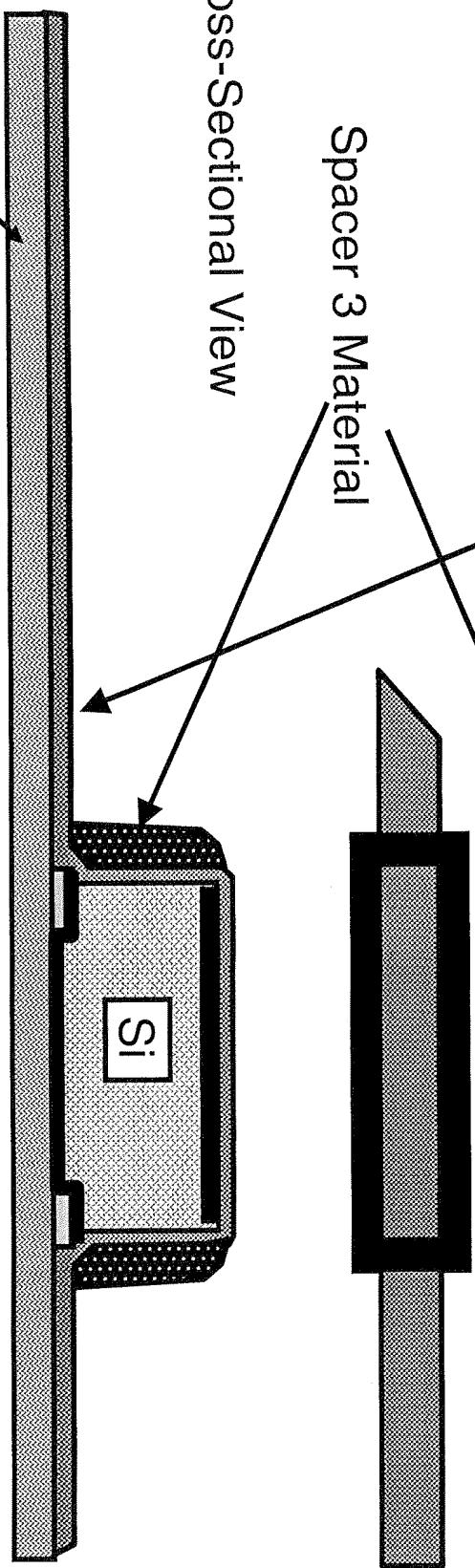


Fig. 7

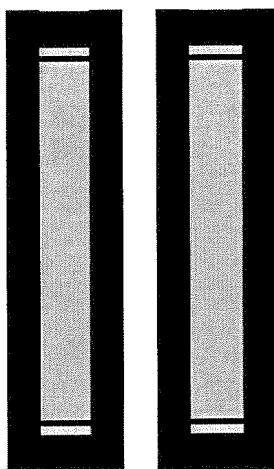
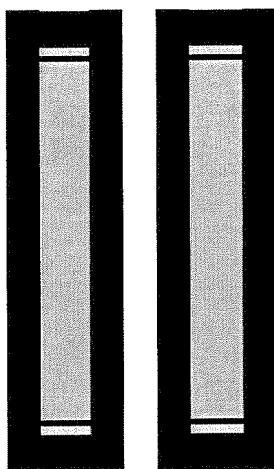
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Grow a thin gate oxide on the Si block, without growing oxide on the catalytic material.

Top View

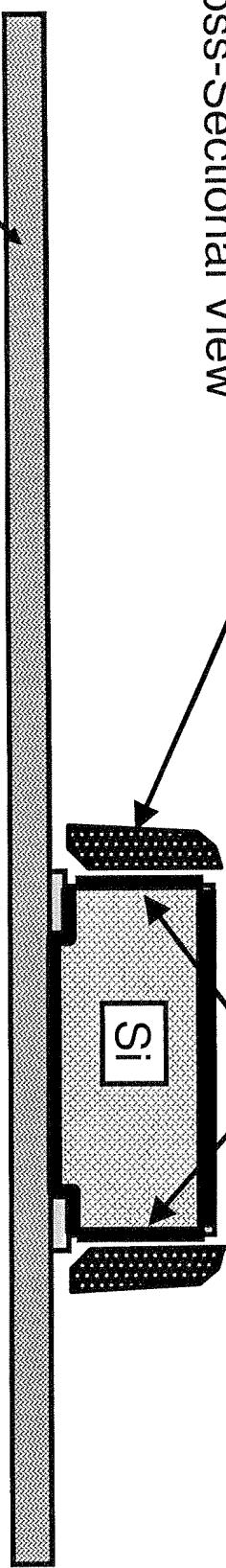


Cross-Sectional View

Spacer 3 Material

Gate Oxide

Si



SiO<sub>2</sub> / Substrate (Si)

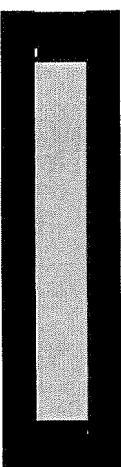
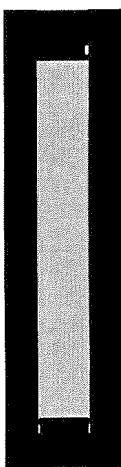
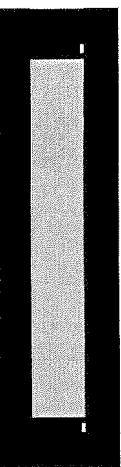
Fig. 8

## Spacer-Defined Nanotube Channel

Grow semiconductor-type carbon nanotubes (CNT) from the catalytic material.

The reactants could feed the CNT reaction at the catalytic material through the space under spacer 3.

Top View



Spacer 3 Material

Cross-Sectional View

CNT Reactants

Gate Oxide

CNT

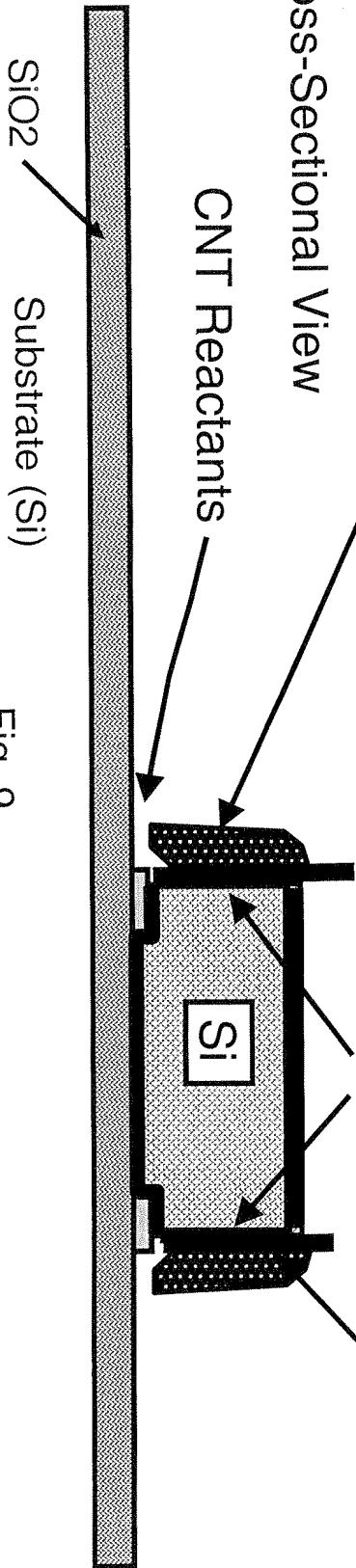
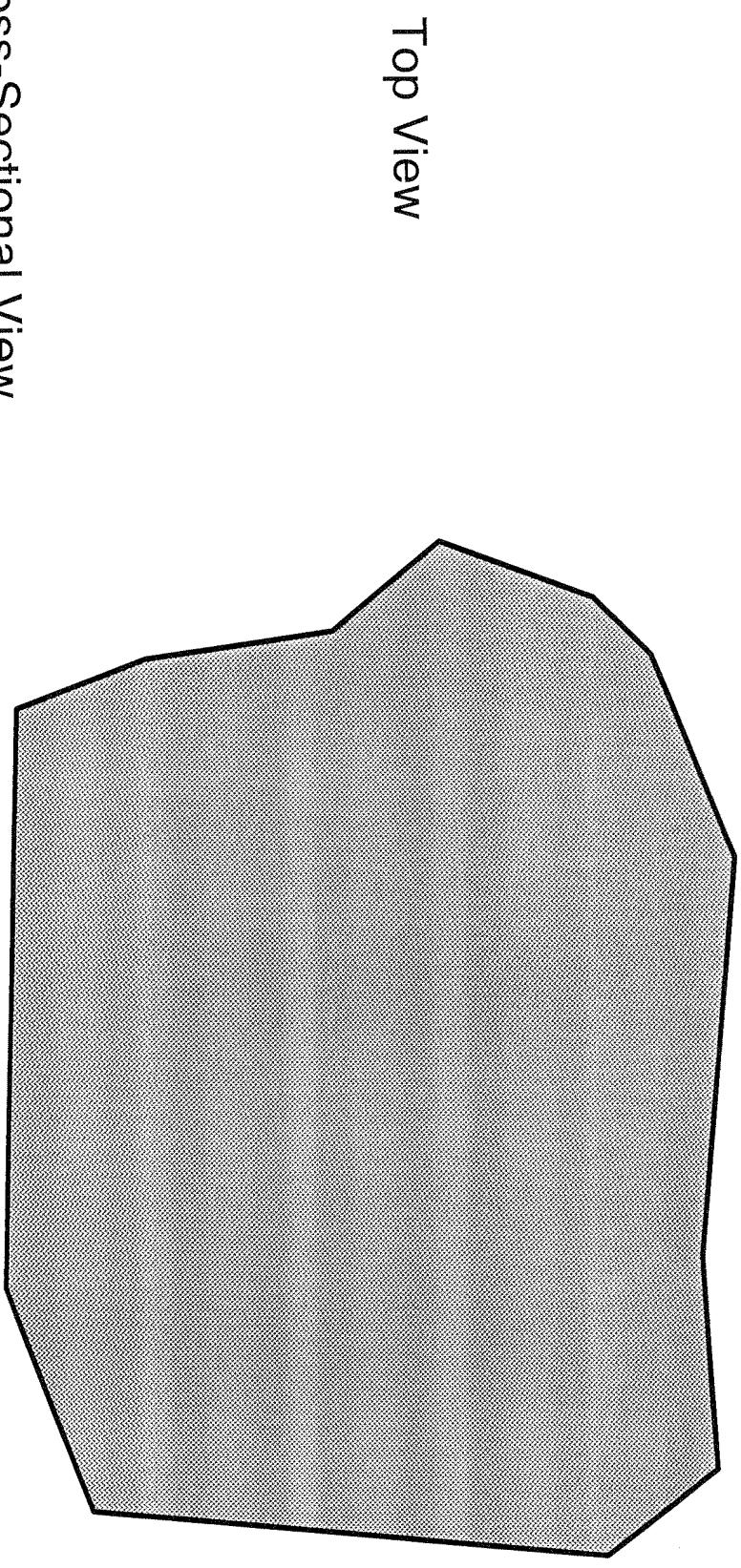


Fig. 9

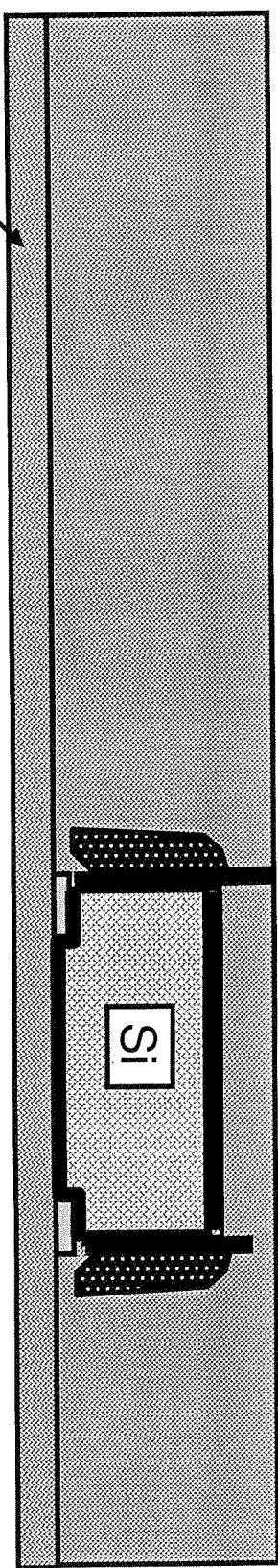
## Spacer-Defined Nanotube Channel

Deposit and planarize an insulating film, e.g. BPSCG.



Top View

### Cross-Sectional View



SiO<sub>2</sub>  
Substrate (Si)

Fig. 10

## Spacer-Defined Nanotube Channel

Etch contact holes to contact the tops of the CNTs.

Fill contact holes with an appropriate metal/conductor & planarize.

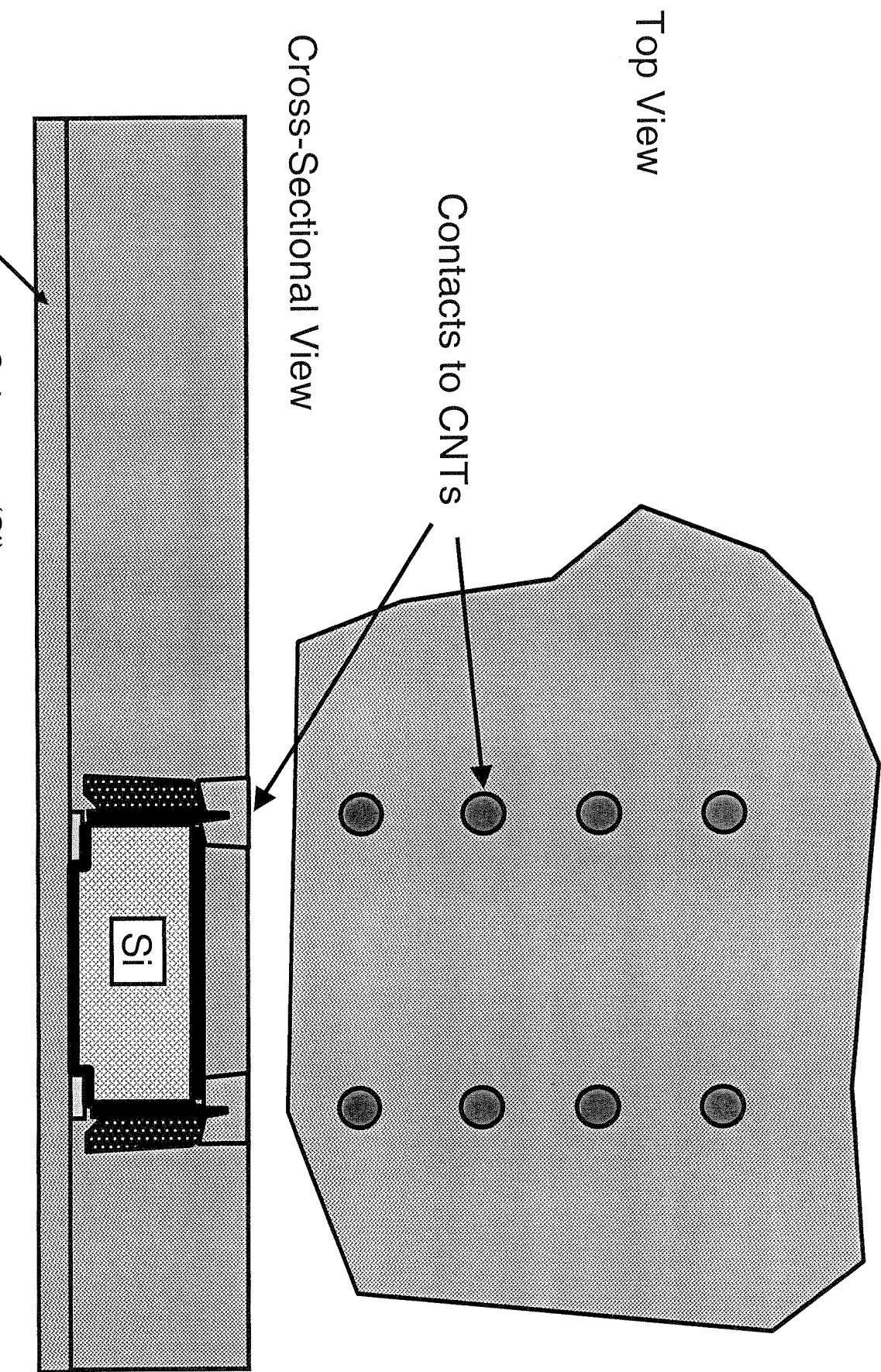


Fig. 11

$\text{SiO}_2$  / Substrate (Si)

## Spacer-Defined Nanotube Channel

### Vertical Carbon Nanotube FET

